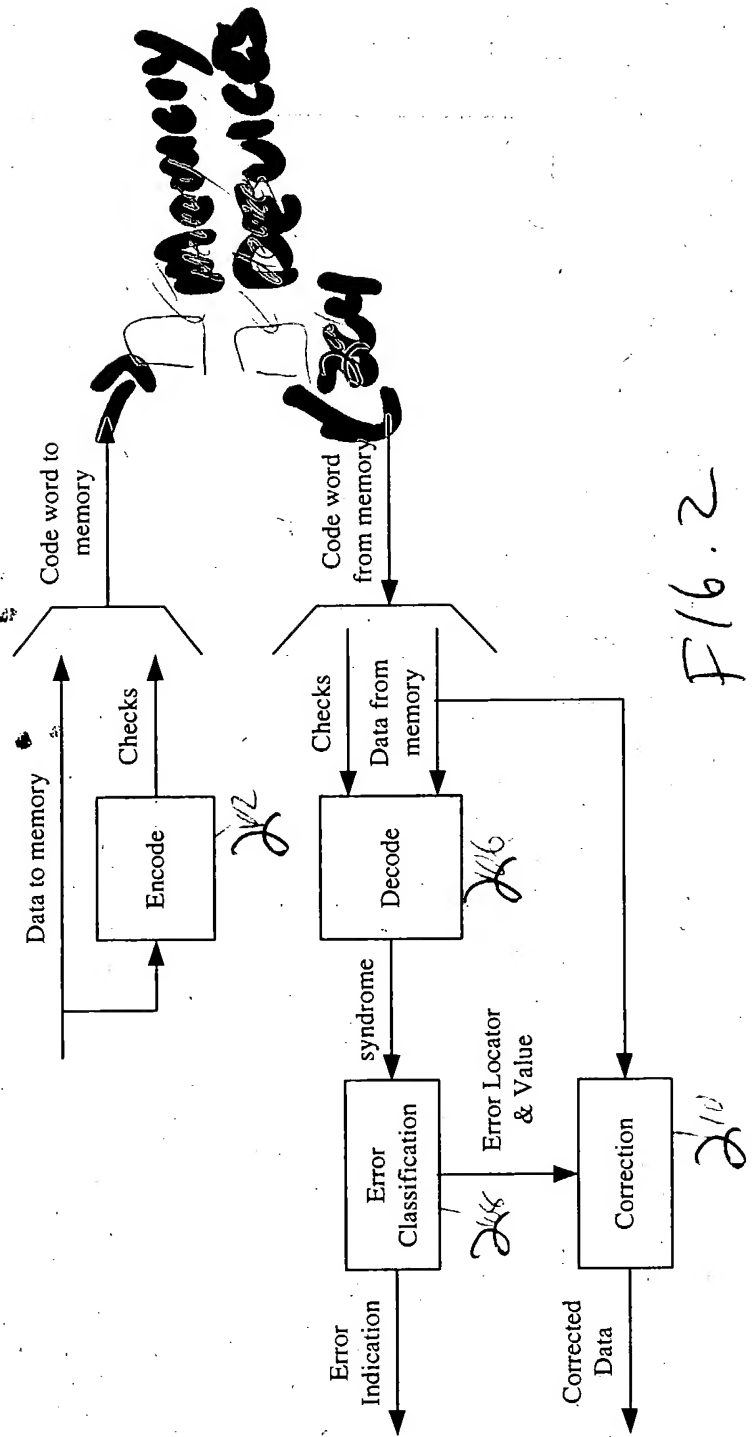


Fig. 1

In the first clock cycle, nibbles n0 and n2 are transferred and mapped to the first nibble of each of two symbols of the



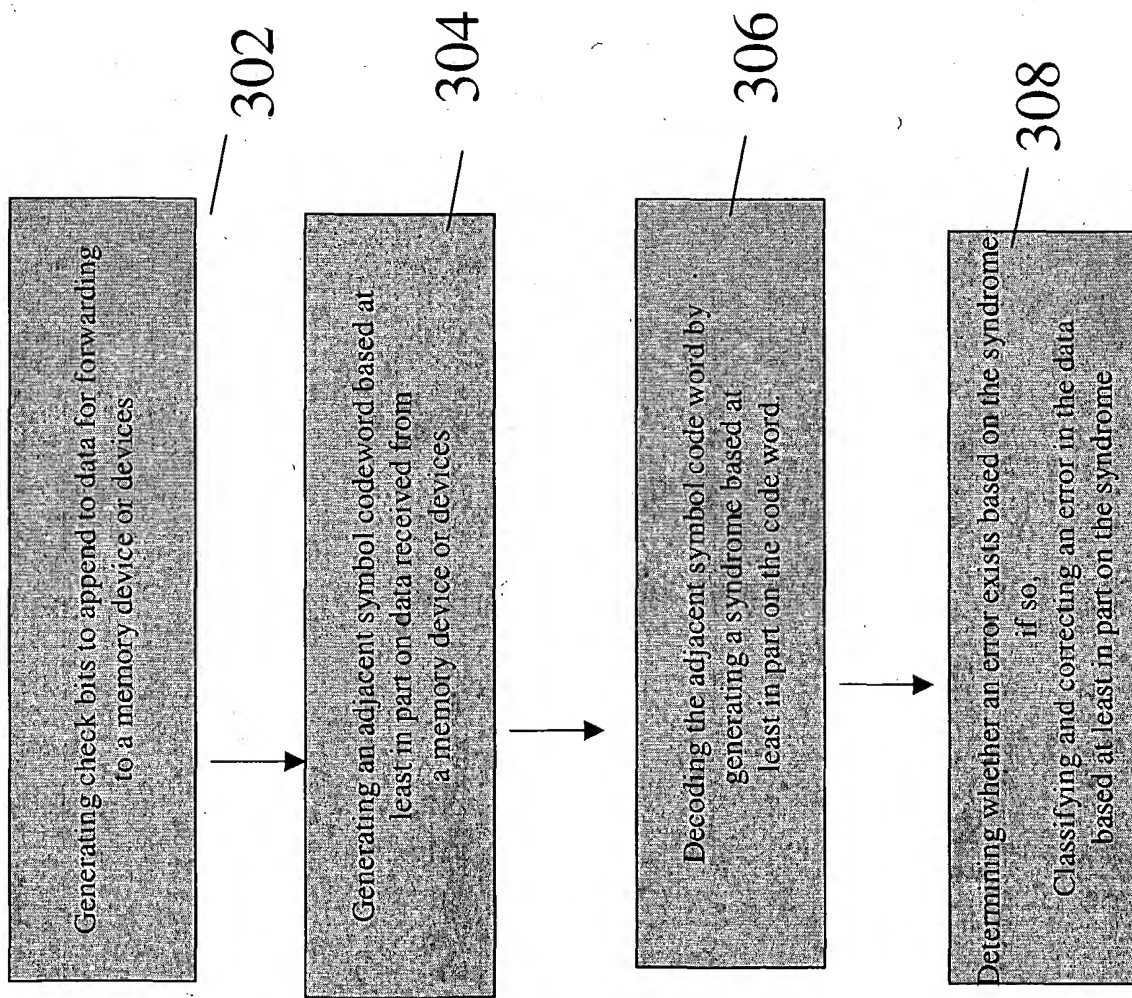


Figure 3

The diagram illustrates a parallel architecture for computing the weight of a node. It consists of a sequence of nodes labeled 0, 1, 2, 3, ..., 17. Each node is connected to a vertical bus. The bus is divided into two sections: the top section is labeled $e_0[0:7]$ and the bottom section is labeled $e_1[0:7]$. Each section is connected to a 'Compute Weight' block. The output of the 'Compute Weight' block for the top section is labeled '402'.

Figure 4

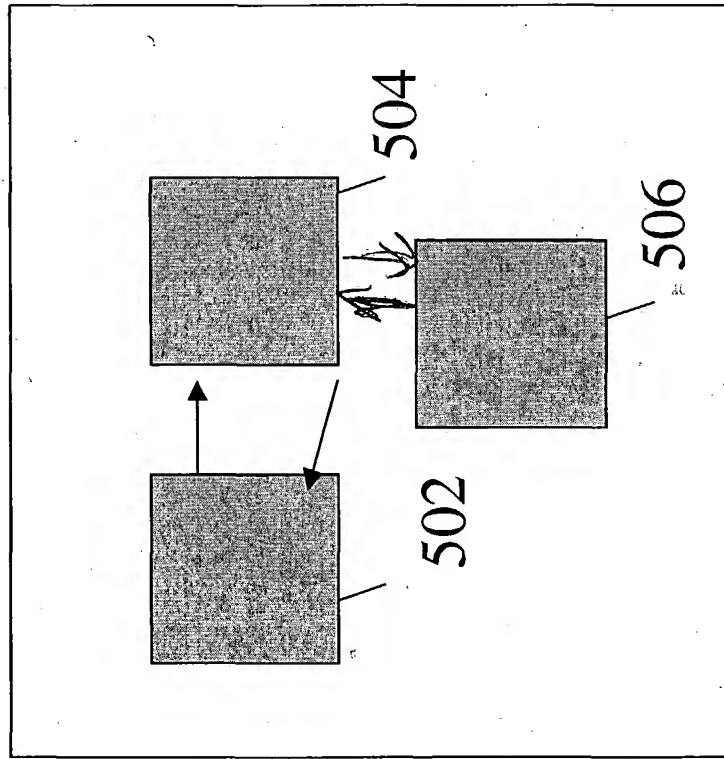


FIGURE 5